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75622.P0001 Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of:

Jerrell P. HEIN

Application No: 09/298,008

Filed: April 22, 1999

For: SUBSCRIBER LINE INTERFACE CIRCUITRY

Examiner: Con P. TRAN

Art Unit: 2644

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Appellant's Brief Under 35 C.F.R. § 1.192

Dear Sir:

Applicant (Appellant) respectfully submits this brief in triplicate in support of an appeal from the Examiner's Final Office Action dated October 23, 2003 that finally rejected claims 1-23. Appellant respectfully requests consideration of this Appeal by the Board of Patent Appeals and Interferences for allowance of the above-referenced application.

The proper time period within which this Brief is required to be filed is two months from the date of receipt of the Notice of Appeal (MPEP § 512). Appellant submitted the Notice of Appeal on February 8, 2004 accompanied by a request for a one month extension of time. The return postcard indicates a receipt date of February 11, 2004 thus establishing a due date of April 11, 2004. This Appeal Brief is accompanied by a two month extension of time thus extending the due date to June 11, 2004. Appellant submits this Brief is timely filed within the time period established by 37 CFR 1.192(a) and extended by 37 C.F.R. § 1.136.

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I. REAL PARTY IN INTEREST

The above-identified application for patent is assigned to Silicon Laboratories, Inc., the real party in interest. Silicon Laboratories, Inc. is a Delaware corporation having a principal place of business in Austin, Texas.

II. RELATED APPEALS AND INTERFERENCES

Appellant is unaware of any other related appeals or interferences that may directly affect or be directly affected by or have a bearing on the Board's decision in this pending appeal.

III. STATUS OF THE CLAIMS

Claims 1-23 are pending. Claims 1-2, 4, 6, 13, 15, and 17 were rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 4,709, 388 of Defretin ("Defretin").

Claims 3 and 14 were rejected under 35 U.S.C. § 103 as being unpatentable over Defretin and U.S. Patent No. 5,926,544 of Zhou ("Zhou").

Claims 5, 7, 16, and 18 were rejected under 35 U.S.C. § 103 as being unpatentable over Defretin in view of U.S. Patent No. 5,854,550 of Knollman ("Knollman").

Claims 8, 9, 19, and 20 were rejected under 35 U.S.C. § 103 as being unpatentable over Defretin in view of Knollman and further in view of U.S. Patent No. 5,881,129 of Chen, et al. ("Chen").

Claims 10-12 and 21-23 were rejected under 35 U.S.C. § 103 as being unpatentable over Defretin in view of U.S. Patent No. 6,263,016 of Bellenger ("Bellenger").

Appellant is appealing the rejection of all of claims 1-23.

IV. STATUS OF AMENDMENTS

Subsequent to the Final Office Action dated October 23, 2003 an Amendment After Final was submitted on December 24, 2003. The Amendment

presented arguments related to the Final Office Action but did not otherwise alter any claims. Claims 1-23 as currently pending are set forth in the attached Appendix I.

V. SUMMARY OF THE INVENTION

Applicant claims a subscriber line interface circuit and its various components. Claims 1-3 are drawn to an integrated circuit that generates linefeed driver control signals in response to sensed tip and ring signals. Claims 4-12 are drawn to a linefeed driver. Claims 13-23 are drawn to an apparatus comprising both an integrated circuit that generates subscriber loop control signals and a linefeed driver responsive to the control signals.

Referring to Figures 1-3, the integrated circuit (signal processor 210) has sense inputs (222) for a sensed tip signal (332, 334) and a sensed ring signal (336, 338) of a subscriber loop (132). The integrated circuit generates control signals (212, 342, 344, 346, 348) for a subscriber loop linefeed driver (220, 310) in response to the sensed signals. The integrated circuit receiving the sensed tip and sensed ring signals performs the appropriate calculations to generate the control signals.

VI. CHARACTERIZATION OF CITED REFERENCES

Defretin discloses a subscriber line interface circuit apparatus having a low tension integrated circuit (CIBT) and a high tension integrated circuit (CIHT). CIHT operates with relatively high voltage (up to 150 V) and CIBT operates solely with low voltages (e.g., up to 10 V). CIHT is an interface circuit for communicating signals on the subscriber line. The low tension integrated circuit CIBT processes signals and controls CIHT. (Defretin, col. 3, lines 1-35; Figs. 1-3). A current measurement circuit 38 residing within the high tension integrated circuit CIHT senses the tip and ring lines and provides a result signal *sd* to the low tension integrated circuit CIBT indicative of the line current. (Defretin, col. 3, line 64-col. 4, line 11). The low tension integrated circuit provides *sc* and *sv* control signals to the high tension integrated circuit. The high tension integrated

circuit controls the tip and ring lines in accordance with the *sc* control signal. The *sv* control signal is used to place the high tension integrated circuit into a low power consumption line monitoring mode.

Zhou, Knollman, Chen, and Bellenger are also directed toward subscriber line interface circuits. Zhou includes a disclosure of a subscriber line interface circuit including an integrated circuit digital signal processor (304) (Zhou, col. 5, lines 1-11; Fig. 3). Knollman discloses a digital subscriber line battery feed circuit providing current and voltage limiting functions for the digital line (Knollman, col. 1, lines 57 - col. 2, line 5). Chen includes a disclosure of a subscriber line interface circuit having microprocessor controlled components to permit isolation of various components for testing without the need for electromechanical relays. (Chen, col. 2, lines 5-50). Bellenger includes a disclosure of circuitry for interfacing a circuit switched subscriber line with a digital packet switched network (Bellenger, col. 5, line 42-col. 6, line 4).

VII. ISSUES PRESENTED

ISSUE 1: Whether claims 1-2 (Group I); 4, 6 (Group II); and 13, 15, and 17 (Group III) were properly rejected under 35 U.S.C. § 102 as being anticipated by Defretin? In particular, does Defretin teach or disclose an integrated circuit having sense inputs for a sensed tip signal and a sensed ring signal of a subscriber loop wherein the same integrated circuit generates linefeed driver control signals in response to the sensed signals?

ISSUE 2: Whether claims 3, 5, 7, 8, 9, 10-12, 14, 16, 18, 19, 20, and 21-23 were properly rejected under 35 U.S.C. § 103 as being unpatentable over Defretin and various combinations of Zhou, Knollman, Chen, and Bellenger.

VIII. GROUPING OF CLAIMS

Claims 1-3 stand together (Group I).

Claims 4-12 stand together (Group II).

Claims 13-23 stand together (Group III).

IX. ARGUMENT

ISSUE 1: Whether claims 1-2 (Group I); 4, 6 (Group II); and 13, 15, and 17 (Group III) were properly rejected under 35 U.S.C. § 102 as being anticipated by Defretin.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)(*see also, In re King*, 231 USPQ 136, 138 (Fed. Cir. 1986)). The identical invention must be shown in as complete detail as is contained in the claim (*Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)).

Appellant respectfully submits that the cited prior art does not teach or disclose an integrated circuit that both a) receives sensed tip and sensed ring signals; AND b) generates a linefeed driver control signal in response to the sensed tip and sensed ring signals.

The Examiner has made a number of inconsistent statements regarding the teachings of Defretin. In particular, the Examiner has made the following statements about Defretin:

1. *Low tension circuit CIBT having sense inputs for a sensed tip signal and a sensed ring signal (sd via 30, 32, 34, 36)* of a subscriber loop, wherein the integrated circuit (by microprocessor) generates a subscriber loop linefeed driver control signal (sc) in response to the sensed signals, wherein the linefeed driver (preamplifiers and output stages 18, 20, 22, 24 respectively of high tension circuit CIHT) does not reside within a same integrated circuit.

(4/10/2003 Office Action, pp 2-3)(*emphasis added*)

2. *Examiner agrees that sd is not the sensed tip current nor the sensed ring current.* The sensed tip current and the sensed ring current are 30, 32, 24, 36. These lines are input to current measurement circuit 38, the result signal sd is sent to low tension integrated circuit (CIBT; col. 3, line 66-col. 4, line 11)

(10/23/2003 Final Office Action, p. 14)(*emphasis added*)

3. Examiner respectfully disagrees. Although sense inputs (30, 32, 24, 36) input to current measurement circuit (38) in which the result signal (sd) is sent to low tension integrated circuit, Defretin still meets the claim limitations since the invention claims are open-

> ended claims. These claims do not exclude the presence of the current measurement circuit (38) between the above sense inputs and low tension integrated circuit. In other words, measurement wires (30, 32, 34, 36) pick up (i.e., sense) signals at output stages (22, 24) of two conductors (10, 12; i.e., tip, ring), bring the signals to current measurement circuit (38), then the signals become signal (sd) that is sent to low tension integrated circuit. Defretin thus discloses all the claimed limitations of independent claims 1, 4, and 13.

(1/29/2004 Advisory Action, pp. 2-3)

The Examiner has not retracted any of these statements. Appellant traverses the Examiner's characterization of Defretin in point 1. Appellant agrees with the Examiner's characterization of Defretin in point 2. Appellant traverses the Examiner's characterization of Defretin in point 3 to the extent it is inconsistent with point 2 and does not accurately reflect the current state of the law or the claims.

The Examiner is free to analogize either Defretin's "high tension" or "low tension" integrated circuit to appellant's claimed integrated circuit. *Appellant respectfully submits, however, that the Examiner has not shown that all the claim limitations are found in either analogy. In short, Defretin does not teach or suggest an integrated circuit that receives sensed tip and ring signals AND generates control signals for the linefeed driver in response to the sensed tip and ring signals* as described in greater detail below.

For example, if Defretin's low tension integrated circuit CIBT is analogized to applicant's claimed integrated circuit, Defretin fails to teach or suggest that the low tension integrated circuit CIBT receives the sensed tip and ring signals as claimed by applicant. To the contrary, Defretin's high tension integrated circuit CIHT clearly senses the tip and ring signals and subsequently provides only a calculated signal *sd* to the low tension integrated circuit CIBT.

If Defretin's "high tension integrated circuit" CIHT is analogized to the claimed integrated circuit, appellant would agree that CIHT receives both the sensed tip and the sensed ring signals. Defretin's CIHT, however, does not generate the linefeed driver control signals. To the contrary, the linefeed driver

control signals (e.g., *sv, sc*) are generated by the low tension integrated circuit CIBT. Moreover, the linefeed driver control signals are generated in response to the result signal *sd* which does not correspond to either the tip or the ring signal.

In an attempt to force the claims to read on the cited reference, the Examiner appears to have analogized Defretin's "low tension circuit" CIBT to appellant's claimed integrated circuit and Defretin's "high tension circuit" CIHT to appellant's claimed linefeed driver. Clearly, Defretin's "low tension circuit" CIBT generates the control signals *sc, sv* for controlling the linefeed driver (i.e., "high tension circuit" CIHT). The only question remaining is whether Defretin's "low tension circuit" CIBT is also receiving the sensed tip and sensed ring signals.

Appellant notes that the tip and ring signals are not sensed or received by the "low tension circuit" CIBT nor does the CIBT have sense inputs for either a sensed tip signal or a sensed ring signal as alleged by the Examiner (*see, e.g.*, Examiner points 1, 3 above).

The Examiner's point 3 is confusing at best. The Examiner is misapplying the appropriate legal standard. The open-endedness of the claims is wholly irrelevant. Each and every element of the claim must be found in Defretin to support a 35 U.S.C. § 102 rejection. The Examiner has acknowledged Defretin's low tension integrated circuit generates control signals responsive to the signal *sd*, however, *sd* is neither the sensed tip signal nor the sensed ring signal and the low tension integrated circuit does not otherwise receive either a sensed tip signal or a sensed ring signal.

Sense inputs 30, 32, 34, 36 for the sensed tip and ring signals *clearly* reside within Defretin's high tension integrated circuit CIHT (Defretin, Fig. 1). None of these sensed signals are provided to the low tension integrated circuit CIBT. Instead, these signals are provided to Defretin's current measuring circuit 38 (residing within the high tension integrated circuit) which generates the signal *sd* for the low tension integrated circuit. (Defretin, col. 3, line 26 - col. 4, line 11). Appellant submits that there is no teaching or suggestion that either the sensed ring signal or the sensed tip signal is provided to Defretin's low tension

integrated circuit. (The Examiner appears to agree with this statement, see, e.g., Examiner's point 2 above).

Referring to col. 4, lines 5-11, Defretin states "In so far as the invention is more particularly concerned, it may be considered that information *sd* is information relating to the fact that the handset has been lifted or replaced at the other end of the line. This information may in fact be obtained by measuring the DC component which may be present in the transverse line current". Appellant submits that at best this suggests that the "current measuring circuit" calculates the transverse line current in order to generate or calculate *sd*. The calculated *sd* is provided to the low tension integrated circuit.

Appellant submits that *sd* is neither the sensed tip current nor the sensed ring current as sometimes alleged by the Examiner. Certainly Defretin does not teach providing both the sensed tip signal and the sensed ring signal to the low tension integrated circuit as alleged by the Examiner.

Applicant respectfully submits that Defretin does not teach or suggest *an integrated circuit having sense inputs for a sensed tip signal and a sensed ring signal of a subscriber loop, wherein the integrated circuit generates a control signal for a subscriber loop linefeed driver in response to the sensed signals, wherein the linefeed driver does not reside within a same integrated circuit.*

In contrast, claim 1 includes the language:

> 1. An integrated circuit package comprising:
> *an integrated circuit having sense inputs for a sensed tip signal and a sensed ring signal of a subscriber loop, wherein the integrated circuit generates a control signal for a subscriber loop linefeed driver in response to the sensed signals, wherein the linefeed driver does not reside within a same integrated circuit.*

(Claim 1)(*emphasis added*)

Similarly, appellant submits *Defretin does not teach or suggest an integrated circuit generating subscriber loop control signals in response to sensed tip and ring signals received by the integrated circuit.*

> 13. An apparatus comprising:
> *an integrated circuit generating subscriber loop control signals in response to a sensed tip signal and a sensed ring signal of a subscriber loop, the sensed tip and ring signals received by the integrated circuit;* and

a linefeed driver for driving a subscriber loop in accordance with the subscriber loop control signals, the linefeed driver providing the sensed tip and ring signals.

(Claim 13)(*emphasis added*)

Claim 4 is directed towards the linefeed driver but inferentially references the integrated circuit with similar language:

4. A subscriber loop linefeed driver comprising:
sense circuitry *providing a sensed tip signal and a sensed ring signal to an integrated circuit, wherein the sensed tip and ring signals correspond to a tip current and a ring current of the subscriber loop;* and
power circuitry for providing battery feed to a ring node and a tip node of a subscriber loop in accordance with *a control signal generated by the integrated circuit in response to the sensed tip and ring signals.*

(Claim 4)(*emphasis added*)

Appellant thus submits that Defretin does not anticipate any of claims 1, 4, or 13 because Defretin fails to teach or disclose each and every element as set forth in the claim. Namely Defretin fails to teach or disclose an integrated circuit that receives the sensed tip and sensed ring signal AND generates the linefeed driver control signal in response to the sensed tip and sensed ring signals.

Claims 2-3 depend from claim 1, claims 5-12 depend from claim 4, and claims 14-23 depend from claim 13. Appellant submits that none of claims 1-3 (Group I), 4-12 (Group II), or 13-23 (Group III) are anticipated under 35 U.S.C. § 102 by Defretin.

Appellant respectfully submits the 35 U.S.C. § 102 rejections have been overcome.

ISSUE 2: Whether claims 3, 5, 7, 8, 9, 10-12, 14, 16, 18, 19, 20, and 21-23 were properly rejected under 35 U.S.C. § 103 as being unpatentable over Defretin and various combinations of Zhou, Knollman, Chen, and Bellenger.

In order to establish a prima facie rejection under 35 U.S.C. § 103, three criteria must be met:

First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference

> teachings. *Second*, there must be a reasonable expectation of success. *Finally*, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure

(*In re Vaeck*, 20 USPQ2d 1438 (Fed. Cir. 1991)(*emphasis added*)

Procedurally, the Examiner must identify the resulting combination and provide a convincing line of reasoning as to why the references should be combined in such a fashion. The Examiner is limited to the use of relevant art for the purposes of an obviousness rejection.

Appellant respectfully submits that the Examiner has failed to establish even a *prima facie* case of obviousness under 35 U.S.C. § 103 and therefore the dependent claims of Groups I-III were improperly rejected under 35 U.S.C. § 103.

Claims 3, 5, 7-12, 14, 16, and 18-23 were rejected as being unpatentable over various combinations of Defretin, Zhou, Knollman, Chen, and Bellenger. None of the rejected claims is an independent claim. Each of the Examiner's rejections relies on Defretin in combination of one or more references.

Appellant disagrees with the Examiner's characterization of Zhou, Knollman, Chen, and Bellenger. Even if appellant agreed, *arguendo*, with the Examiner's assessment of these references, appellant notes that the Examiner is still relying on combining these references with Defretin in order to teach all the claim limitations. However, Zhou, Knollman, Chen, and Bellenger fail to make up for the deficiencies of Defretin whether taken alone or in combination.

Thus, alone or combined, the references fail to teach all the claim limitations. Namely, none of these references alone or in combination teaches or suggests an integrated circuit that receives a sensed tip signal and a sensed ring signal AND generates a linefeed driver control signal responsive to the sensed tip signal and the sensed ring signal. The Examiner is relying upon Defretin in both the § 102 and §103 rejections for the teaching of these elements.

The patentability of independent claims 1, 4, and 13 in view of Defretin has been argued above and Zhou, Knollman, Chen, and Bellenger have not been asserted against any independent claims. Appellant submits that if an independent claim is nonobvious under 35 U.S.C. § 103, then any claim

depending therefrom is nonobvious. (see MPEP § 2143.03 citing *In re Fine*, 5 USPQ2d 1596 (Fed. Cir. 1988)).

Given that independent claims 1, 4, and 13 are patentable over Defretin for the reasons cited above (and that no rejection of any independent claim under 35 U.S.C. § 103 has been asserted and the remaining references fail to make up for the deficiencies of Defretin), appellant submits that dependent claims 2-3, 5-12, and 14-23 are patentable under 35 U.S.C. § 103 in view of the cited references. Accordingly, appellant submits that all of claims 1-23 are patentable under 35 U.S.C. § 103 in view of the cited references.

Appellant submits that the rejections under 35 U.S.C. § 103 have been overcome.

X. CONCLUSION

Appellant respectfully submits that the stated rejections cannot be maintained in view of the arguments set forth above. No single reference expressly or inherently discloses each and every element set forth in *any* of the claims. Thus the rejection under 35 U.S.C. § 102 is without merit. The Examiner has failed to establish even a *prima facie* case of obviousness under 35 U.S.C. § 103 because *the references alone or combined still fail to teach all the claim limitations of any claim.* Thus the rejections under 35 U.S.C. § 103 are similarly without merit.

Appellant respectfully submits that all of claims 1-23 (Groups I, II, and III) are patentable under 35 U.S.C. § § 102, 103 in view of the cited references and requests that the Board of Patent Appeals and Interferences direct allowance of the rejected claims.

If there are any issues that can be resolved by telephone conference, the undersigned representative of the appellant may be contacted at **(512) 306-9470.**

Respectfully submitted,

Date: June 9, 2004

William D. Davis
Reg. No. 38,428

APPENDIX I

Pending claims 1-23 read as follows:

1. An integrated circuit package comprising:

an integrated circuit having sense inputs for a sensed tip signal and a sensed ring signal of a subscriber loop, wherein the integrated circuit generates a control signal for a subscriber loop linefeed driver in response to the sensed signals, wherein the linefeed driver does not reside within a same integrated circuit.

2. The integrated circuit package of claim 1 wherein the sensed tip signal includes first and second sampled tip voltages, wherein a difference between the first and second sampled tip voltages is proportional to the tip current, wherein the sensed ring signal includes first and second sampled ring voltages, wherein a difference between the first and second sampled ring voltages is proportional to the ring current.

3. The integrated circuit package of claim 1 wherein the integrated circuit is a complementary metal oxide semiconductor (CMOS) integrated circuit.

4. A subscriber loop linefeed driver comprising:

sense circuitry providing a sensed tip signal and a sensed ring signal to an integrated circuit, wherein the sensed tip and ring signals correspond to a tip current and a ring current of the subscriber loop; and

power circuitry for providing battery feed to a ring node and a tip node of a subscriber loop in accordance with a control signal generated by the integrated circuit in response to the sensed tip and ring signals.

5. The subscriber loop linefeed driver of claim 4 wherein the sense circuitry comprises:

a tip resistor series-coupled to the tip node and the power circuitry;

a pair of tip sampling resistors one end of each tip sampling resistor connected to opposite ends of the tip resistor, the other end of each tip sampling resistor forming a tip sense node;

a ring resistor series-coupled to the ring node and the power circuitry;

a pair of ring sampling resistors one end of each ring sampling resistor connected to opposite ends of the ring resistor, the other end of each ring sampling resistor forming a ring sense node.

6. The subscriber loop linefeed driver of claim 4 wherein the sensed tip signal comprises first and second sampled tip voltages, wherein a difference between the first and second sampled tip voltages is proportional to the tip current, wherein the sensed ring signal includes first and second sampled ring voltages, wherein a difference between the first and second sampled ring voltages is proportional to the ring current.

7. The subscriber loop linefeed driver of claim 4 wherein the power circuitry comprises:

a tip control circuit, wherein the tip control circuit increases a tip node voltage in response to a first tip control signal, wherein the tip control circuit decreases a tip node voltage in response to a second tip control signal; and

a ring control circuit wherein the ring control circuit increases a ring node voltage in response to a first ring control signal, wherein the ring control circuit decreases a ring node voltage in response to a second ring control signal.

8. The subscriber loop linefeed driver of claim 7 wherein the tip control circuit comprises:

a first transistor of a first type having an emitter coupled to receive the first tip control signal;

a second transistor of the first type having an emitter coupled to receive the second tip control signal, wherein a base of each of the first and second transistors is coupled to first node;

a third transistor of a second type having a collector coupled to a collector of the first transistor and an emitter coupled to a second node;

a resistor having a first end coupled to the second node, a second end of the resistor coupled to a base of the third transistor and a collector of the second transistor.

9. The subscriber loop linefeed driver of claim 8 wherein the first type is a PNP bipolar junction transistor, wherein the second type is an NPN bipolar junction transistor.

10. The subscriber loop linefeed driver of claim 4 further comprising:

voiceband circuitry for bi-directional communication of voiceband data between the ring and tip nodes and a voiceband data interface, wherein the voiceband circuitry provides the analog voiceband data interface with d.c. isolation from the ring and tip nodes.

11. The apparatus of claim 10 wherein the voiceband circuitry further comprises:

a first voiceband data output node;

a load coupled to the first voiceband data output node;

a first voiceband data input node, wherein the load and the first voiceband data input node are capacitively coupled to a selected one of the tip and ring nodes.

12. The apparatus of claim 4 further comprising voiceband circuitry for bi-directional communication of voiceband data between the ring and tip nodes and a voiceband data interface, wherein the voiceband circuitry further comprises:

a first voiceband data input node capacitively coupled to a selected one of the ring and tip nodes for receiving voiceband data from the subscriber loop, wherein voiceband data transmitted to the subscriber loop is superimposed on the linefeed control signals.

13. An apparatus comprising:

an integrated circuit generating subscriber loop control signals in response to a sensed tip signal and a sensed ring signal of a subscriber loop, the sensed tip and ring signals received by the integrated circuit; and

a linefeed driver for driving a subscriber loop in accordance with the subscriber loop control signals, the linefeed driver providing the sensed tip and ring signals.

14. The apparatus of claim 13 wherein the integrated circuit is a complementary metal oxide semiconductor (CMOS) integrated circuit.

15. The apparatus of claim 13 wherein the linefeed driver comprises:

power circuitry for providing battery feed to a ring node and a tip node of a subscriber loop in accordance with a linefeed control signal; and

sense circuitry providing a sensed tip signal and a sensed ring signal, wherein the sensed tip and ring signals correspond to a tip current and a ring current of the subscriber loop.

16. The linefeed driver of claim 15 wherein the sense circuitry comprises:

a tip resistor series-coupled to the tip node and the power circuitry;

a pair of tip sampling resistors one end of each tip sampling resistor connected to opposite ends of the tip resistor, the other end of each tip sampling resistor forming a tip sense node;

a ring resistor series-coupled to the ring node and the power circuitry;

a pair of ring sampling resistors one end of each ring sampling resistor connected to opposite ends of the ring resistor, the other end of each ring sampling resistor forming a ring sense node.

17. The linefeed driver of claim 15 wherein the sensed tip signal comprises first and second sampled tip voltages, wherein a difference between the first and second sampled tip voltages is proportional to the tip current, wherein the sensed ring signal includes first and second sampled ring voltages, wherein a difference between the first and second sampled ring voltages is proportional to the ring current.

18. The linefeed driver of claim 15 wherein the power circuitry comprises:

a tip control circuit, wherein the tip control circuit increases a tip node voltage in response to a first tip control signal, wherein the tip control circuit decreases a tip node voltage in response to a second tip control signal; and

a ring control circuit wherein the ring control circuit increases a ring node voltage in response to a first ring control signal, wherein the ring control circuit decreases a ring node voltage in response to a second ring control signal.

19. The linefeed driver of claim 18 wherein the tip control circuit comprises:

a first transistor of a first type having an emitter coupled to receive the first tip control signal;

a second transistor of the first type having an emitter coupled to receive the second tip control signal, wherein a base of each of the first and second transistors is coupled to first node;

a third transistor of a second type having a collector coupled to a collector of the first transistor and an emitter coupled to a second node; and

a resistor having a first end coupled to the second node, a second end of the resistor coupled to a base of the third transistor and a collector of the second transistor.

20. The linefeed driver of claim 19 wherein the first type is a PNP bipolar junction transistor, wherein the second type is an NPN bipolar junction transistor.

21. The linefeed driver of claim 15 further comprising:

voiceband circuitry for bi-directional communication of voiceband data between the ring and tip nodes and a voiceband data interface, wherein the voiceband circuitry provides the analog voiceband data interface with d.c. isolation from the ring and tip nodes.

22. The linefeed driver of claim 21 wherein the voiceband circuitry further comprises:

a first voiceband data output node;

a load coupled to the first voiceband data output node; and

a first voiceband data input node, wherein the load and the first voiceband data input node are capacitively coupled to a selected one of the tip and ring nodes.

23. The apparatus of claim 15 further comprising voiceband circuitry for bi-directional communication of voiceband data between the ring and tip nodes and a voiceband data interface, wherein the voiceband circuitry further comprises:

a first voiceband data input node capacitively coupled to a selected one of the ring and tip nodes for receiving voiceband data from the subscriber loop, wherein voiceband data transmitted to the subscriber loop is superimposed on the linefeed control signals.